2015–1293

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

RICKY D. HANGARTNER,

Plaintiff–Appellant,

v.

INTEL CORPORATION,

Defendant–Appellee.

Appeal from the United States District Court for the District of Oregon in case No. 3:14-cv-00141-MO, Judge Michael W. Mosman

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BRIEF OF APPELLEE INTEL CORPORATION

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July 20, 2015

CERTIFICATE OF INTEREST

Counsel for appellee Intel Corporation certifies the following:

The full name of every party represented by me is:

Intel Corporation

The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

n/a

The names of all parent corporations and any publicly held companies that own 10% or more of the stock of the party represented by me are:

n/a

The names of all law firms and the partners or associates who appeared for the party or amicus curiae now represented by me in the trial court or are expected to appear in this Court are listed below.

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Dated: July 20, 2015

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BPAI	Board of Patent Appeals and Interferences of the PTO
Dr. Hangartner	appellant Ricky D. Hangartner, Ph.D., named inventor on the '422 patent
Intel	appellee Intel Corporation
PTO	United States Patent and Trademark Office
'422 patent	U.S. Patent No. 6,463,422 B1
'422(*xx*:*yy*-*zz*)	column *xx*, lines *yy* to *zz* of the '422 patent
'518 patent	U.S. Patent No. 5,560,518

RELATED CASES

Intel and its counsel are unaware of any other appeals in or from the same civil action that have previously been before this or any other appellate court. Intel and its counsel are likewise unaware of any cases pending in this or any other court that will directly affect or be directly affected by the decision in this case.

INTRODUCTION

This case reduces to one issue: whether the sole asserted claim requires a circuit with multiple logic elements, such that a circuit with only one logic element cannot infringe. Intel contends that the district court correctly construed the claim to require multiple logic elements and correctly entered summary judgment of noninfringement.

Claim 1 of the '422 patent recites a logic circuit for generating random values that form a proposed solution to a computing problem. What Dr. Hangartner calls "limitation (a)" of claim 1 provides that the circuit includes one logic element for generating a random value per variable of a problem to be solved and specifies certain required components. "Limitation (b)" recites that the circuit further comprises a

> common synchronization means coupled to all of the nondeterministic logic elements for synchronizing operation of the nondeterministic logic elements.

The claimed "synchronizing operation" of the logic elements refers to simultaneously prompting all of the logic elements to collectively generate a set of random values. This set of random values forms a complete "guess" to a complex computing problem, the type of problem the system of the '422 patent was intended to solve. Synchronization among ele-

ments is necessary to ensure that the elements act as a unit: unless each element generates its own random value together with all the others, there will be no solution to check.

Dr. Hangartner asserts that this claim can include only a single logic element. He relies on limitation (a) for this proposition, arguing that because part of it uses singular language, "all of the logic elements" in limitation (b) should be read to mean "all of the *one or more* logic elements." Dr. Hangartner is wrong, because limitation (a) simply characterizes the function and components of each logic element. There is no reasonable way to reconcile the concepts of limitation (b)—which requires a "common" means that "synchronizes" "all of the" logic elements—with a single-element circuit, particularly in light of the intrinsic record.

And even if the claim language left any doubt that claim 1 requires multiple logic elements, the prosecution history puts this to rest. As originally filed, the predecessor of claim 1 recited only limitation (a), the limitation Dr. Hangartner argues can cover a single logic element. The PTO rejected that claim for double patenting. Dr. Hangartner added limitation (b) to overcome this rejection, thus *conceding* that a

single-element circuit was *not* patentable without the additional requirement of multiple such logic elements, all synchronized in operation. Dr. Hangartner now contends that limitation (b) means only that each element must "operate properly"—but if that were true, the amendment would not have been sufficient to overcome the rejection.

The district court correctly construed claim 1 as requiring synchronization of more than one logic element. Because Dr. Hangartner conceded that the accused Intel products do not include multiple logic elements, judgment of noninfringement followed directly from the court's claim construction. The Court should affirm that judgment.

STATEMENT OF ISSUES

1. "Limitation (b)" of claim 1 requires a "common synchronization means coupled to all of the nondeterministic logic elements for synchronizing operation of the nondeterministic logic elements." The district court agreed with Intel that "synchronizing" "all of the … logic elements" in "common" requires synchronizing *multiple* "logic elements," and rejected Dr. Hangartner's argument that a circuit with "one or more" logic elements falls within the scope of the claim. The plain language of claim 1, the prosecution history, and the specification each

support this construction. Should this Court affirm the district court's construction and the resulting judgment of noninfringement?

STATEMENT OF THE CASE

I. The Computing System of the '422 Patent Generates Sets of Random Numbers as "Guesses" for Solving Complex Computing Problems.

As Dr. Hangartner recognizes (at 5, 19), the '422 patent discloses a system for solving complex computing problems. The patent focuses particularly on Nondeterministic Polynomial Time complete ("NP-complete") problems, a class of problems that cannot be efficiently solved using algorithms or rules. '422(1:14-16). Because "no efficient solution method is known" for these problems, Dr. Hangartner theorized that the fastest way to solve an NP-complete problem was to generate a random "guess," test that solution, and generate another guess if the first (or second, or millionth) is wrong. '422(3:66-4:3). Each "guess" consists of a set of random binary values, one value for each variable of the problem. '422(4:6-8). The '422 patent refers to such randomly-generated values as "probabilistic variables." '422(4:8-10).

Various techniques for generating random values were known before the '422 patent's priority date. One technique used a logic circuit

called a "latch"—a pair of transistor inverter circuits arranged in a cross-coupled form—to generate random numbers based on internal circuit noise. This technique was disclosed by the prior art Bellido reference, which was cited during prosecution of the parent of the '422 patent. A259, A406 (rejecting claims of the application that issued as the '518 patent because "Bellido discloses a circuit description for a random number generator which comprises a cross coupled pair of inverting gates, and means for equalizing charge in each cross coupled pair of inverting gates"). Dr. Hangartner sought to extend random number generation to larger-scale problems, with the goal of "allow[ing] solution of computing problems that heretofore could not be practically solved in small systems." '422(2:7-9).

To this end, the computing system of the '422 patent includes a "Nondeterministic ('ND') subsystem consisting of a set of ND elements." '422(4:12-13).[1] These logic elements generate sets of random values as guesses to a computing problem stored in memory. Testing

[1] "Nondeterministic" effectively means "random." Intel agrees with Dr. Hangartner (at 10 n.1) that the issue on appeal does not turn on the use or meaning of "nondeterministic" and that it need not be repeated with every reference to the logic elements.

circuitry then "quickly checks whether [the] set of values (i.e. a proposed solution) satisfies the problem presented." '422(4:15-19). If not, the logic subsystem generates a new set of random values. '422(2:26-32).

This *synchronized* use of logic elements was Dr. Hangartner's attempt to go beyond the known techniques for generating single random binary values. The specification teaches that "*[t]he present invention* is most useful for solving a combinatorial computing problem having a large number of variables"—for example, "a computing problem [with] 1000 independent variables." '422(3:60-63) (emphasis added).

A. The Logic Subsystem of the '422 Patent Includes a "Series" of Synchronized Logic Elements that Generate Random Values.

Figure 4 depicts an example of the '422 patent's multiple-element logic subsystem:

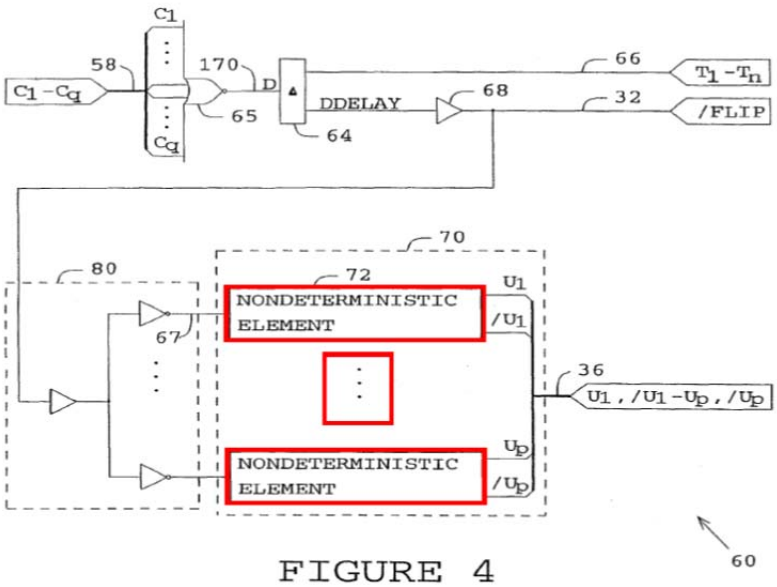


FIGURE 4

The subsystem "includes a *series* of p individual … logic elements **70**." '422(7:1-2) (emphasis added); *see also* '422(2:37-38) ("The nondeterministic subsystem includes a series of semiconductor nondeterministic logic elements."). This series of p logic elements is highlighted in red in Figure 4, above; the ellipsis indicates that an undefined number of additional logic elements is included between the first and p^{th} element. "One ND element is provided for each probabilistic variable" in the problem to be solved. '422(4:15-16); *see also* claim 1, *infra* at 11 ("one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables").

Each logic element includes a cross-coupled pair of transistors (a latch) that "generat[es] a respective one of the random … values of the

series of variables [in the computing problem]." '422(2:38-42). Thus, "[e]ach individual ND logic element … generates one of the probabilistic variables and its complement." '422(7:3-5); *see also* '422(4:16-17). The random values are output in parallel on bus **36** and tested to see if the "guess" forms a solution to the stored problem. '422(7:6-7, 5:54-60, 6:12-22, 6:57-59).

1. A "Synchronization Signal" Simultaneously Prompts All of the Logic Elements to Generate A New Set of Values.

If the set of values is not a solution, the logic elements are "synchronized" by a "synchronization signal" that simultaneously prompts all of the elements to collectively generate a new set of random values. More particularly, if the values previously generated by the logic elements are not a solution to the problem, signal D (element **170** in Figure 4) is low. '422(11:5-6). Signal D is input to delay circuit **64**, which generates a DDELAY signal that, "through a buffer **68**, provides the synchronization signal /FLIP **32**." '422(6:63-67).

When DDELAY is low, it causes "/FLIP [to go] high, to synchronize and begin a new [computation] cycle." '422(11:5-7); *see so* '422(5:12-13); '422 Fig. 12. The /FLIP signal **32** then "fans out … to

form a series of control signals," each of which is "coupled to a corresponding one of the individual ND elements." '422(7:8-11). The synchronization signal path is highlighted in red in Figure 4, reproduced below:

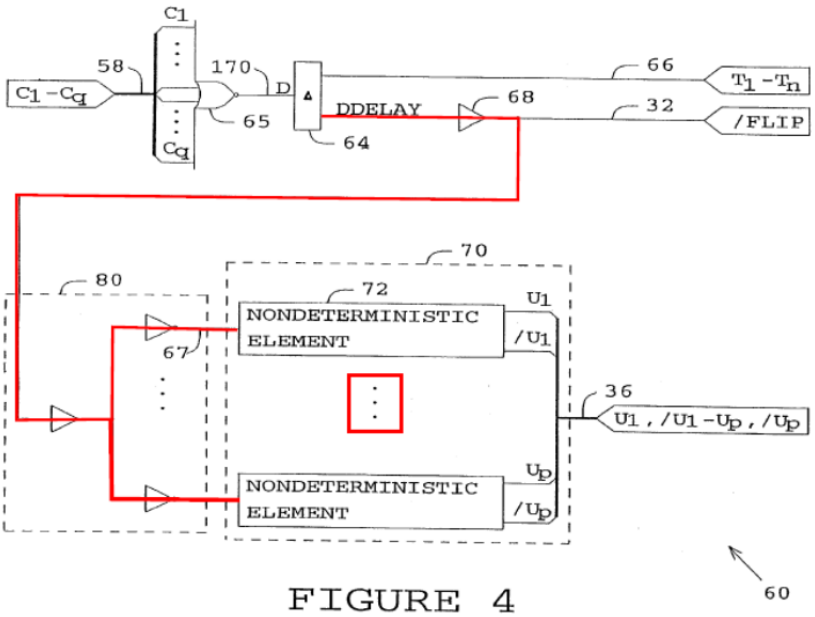


FIGURE 4

By using a signal common to all of the logic elements, signal **32**, to synchronize their operation, the logic circuit of the '422 patent ensures that all elements are simultaneously prompted to generate random values upon each new cycle.

2. Claim 1 Recites a Logic Element for Each Problem Variable and a "Common Synchronization Means Coupled to All of the … Logic Elements."

The '422 patent recites three independent claims. Claim 1 is directed to the nondeterministic subsystem: it recites a logic circuit that includes one logic element for each variable of the computing problem and a "common synchronization means coupled to all of the nondeterministic logic elements."

Claims 2 and 8 incorporate this multi-logic element subsystem into a system that includes a stored representation of the specific computing problem to be solved. The end-to-end "hardware probabilistic computing system" recited by these claims includes the memory that stores the predetermined computing problem, the multi-element nondeterministic subsystem that generates a set of random values (*i.e.*, the logic circuit of claim 1), testing circuitry that indicates whether the set of random values satisfies the problem, and a "feedback means" that asserts "flip signal [**32**]" if not. '422(13:13-58, 14:39-15:45).

Dr. Hangartner asserted only claim 1 against Intel. Claim 1 reads as follows:

A nondeterministic logic circuit for generating random boolean values of one or more variables as a proposed solution to a computing problem expressed in conjunctive normal form as one [or] more clauses in said one or more variables, the logic circuit comprising:

[(a)] one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables; and

each nondeterministic logic element comprising:

a cross-coupled pair of transistor inverter circuits;

means for controlling power to the cross-coupled pair of transistor inverter circuits; and

means for equalizing charge on the gates of the transistor inverter circuits while power is removed from the cross-coupled pair, thereby driving the cross-coupled pair to an unstable equilibrium, whereby intrinsic circuit noise will cause the cross-coupled pair to randomly assume one of two stable states when power is restored to the cross-coupled pair, the stable state assumed by the cross-coupled pair providing a probabilistically selected random boolean value

[(b)] and further comprising ***common synchronization means coupled to all of the nondeterministic logic elements for synchronizing operation of the nondeterministic logic elements***.

'422(12:54-13:12) (Dr. Hangartner's (a) and (b) and emphasis added).

B. Dr. Hangartner Added the "Common Synchronization Means" Limitation (b) During Prosecution to Overcome a Rejection.

As filed, the claim that issued as claim 1—claim 9 in the original application—recited only limitation (a). Limitation (b) was recited by application claim 10, which depended from application claim 9. A209, A214.

The examiner rejected application claim 9 for statutory-type double patenting based on claim 1 of the parent of the '422 patent, U.S. Patent No. 5,680,518 ("the '518 patent"). This claim is shown below, along with application claims 9 and 10 as originally filed. Language highlighted in gray is identical between the claims:

'518 Patent	Application Issued as the '422 Patent (as originally filed)
1. A nondeterministic logic circuit for generating random boolean values of one or more variables for use a proposed solution to a computing problem expressed in conjunctive normal form as one more clauses in said one or more variables, the logic circuit comprising:	9. A nondeterministic logic circuit for generating random boolean values of one or more variables for use a proposed solution to a computing problem expressed in conjunctive normal form as one more clauses in said one or more variables, the logic circuit comprising:
one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables: and	one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables; and
each nondeterministic logic element comprising:	each nondeterministic logic element comprising:
a cross-coupled pair of transistor inverter circuits;	a cross-coupled pair of transistor inverter circuits;

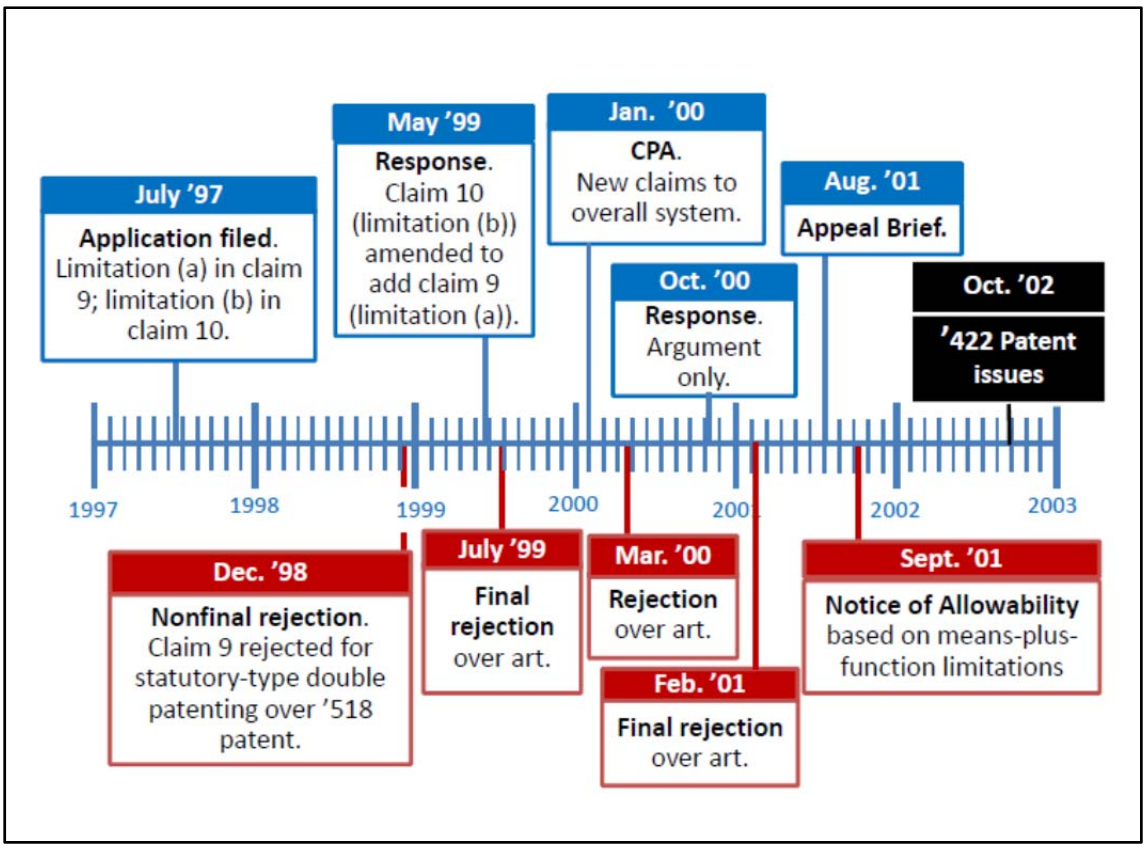
'518 Patent	Application Issued as the '422 Patent (as originally filed)
means for controlling power to the cross-coupled pair of transistor inverter circuits; and	means for controlling power to the cross-coupled pair of transistor inverter circuits; and
means for equilizing [sic] charge on the gates of the transistor inverter circuits while power is removed from the cross-coupled pair, thereby driving the cross-coupled pair to an unstable equilibrium, whereby intrinsic circuit noise will cause the cross-coupled pair to randomly assume one of two stable states when power is restored to the cross-coupled pair, the stable state assumed by the cross-coupled pair providing a probabilistically selected random boolean value, and	means for equilizing [sic] charge on the gates of the transistor inverter circuits while power is removed from the cross-coupled pair, thereby driving the cross-coupled pair to an unstable equilibrium, whereby intrinsic circuit noise will cause the cross-coupled pair to randomly assume one of two stable states when power is restored to the cross-coupled pair, the stable state assumed by the cross-coupled pair providing a probabilistically selected random boolean value.
wherein at least one of the nondeterministic logic elements further comprises means for receiving and storing a logic bit having a predetermined boolean value so that the corresponding variable value is predetermined.	10. A nondeterministic logic circuit according to claim 10 [sic] and further comprising common synchronization means coupled to all of the nondeterministic logic elements for synchronizing operation of the nondeterministic logic elements.

As shown above, the entirety of application claim 9 was already present in claim 1 of the '518 patent. Claim 1 of the '518 patent recited "one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables" and specified the same subcomponents responsible for "providing [the] … random boolean value"—a latch, power means, and charge equalization means. Claim 1 of the '518 patent also recited a means for receiving and storing

a predetermined value for a variable. Claim 1 did not, however, recite a common synchronization means for synchronizing the operation of multiple logic elements.

To overcome the double-patenting rejection, Dr. Hangartner re-wrote application claim 10 in independent form to include the limitations of application claim 9 and canceled claim 9. A209-10, A214. As a result, application claim 10 recited limitations (a) and (b)—one logic element for each variable, with a common synchronization means that synchronized the operation of all logic elements. The addition of limitation (b) is what overcame the double patenting rejection.

Dr. Hangartner made no further changes to the language of application claim 10. The examiner still issued a series of rejections based on the prior art, ultimately issuing a final rejection of all claims on obviousness grounds. Dr. Hangartner filed an appeal brief with the Board of Patent Appeals and Interferences (BPAI) challenging these rejections. While that was pending, the examiner issued a notice of allowability *sua sponte*, citing the limiting nature of the claims' means-plus-function limitations. The following figure outlines these prosecution events:



Application claim 10 was renumbered as claim 1 when the '422 patent issued.

Dr. Hangartner relied on the significance of the added "common synchronization means" limitation (b) throughout prosecution. For example, in his appeal brief to the BPAI, Dr. Hangartner characterized what became claim 1 as

> includ[ing] essentially two elements: (a) one nondeterministic logic element for each variable, to generate a random boolean value for the corresponding variable; and (b) a 'common synchronization means' that synchronizes operation of the nondeterministic logic *elements*.

> *They* have to be synchronized because each guess at a solution to the problem requires that a random value be picked *for every variable* in the problem.

A220 (emphases added). Thus, Dr. Hangartner represented to the PTO that the claimed "synchronization" occurred between separate logic elements: the elements had to be "synchronized"—that is, all elements simultaneously made to generate a random number—to ensure that random values were generated for all of the problem variables. He also focused on his invention's ability to solve complex computing problems. *See, e.g.*, A219 ("*The invention* can be briefly summarized as an electronic system specially configured to solve certain types of difficult (technically called 'NP-complete') computing problems.") (emphasis added).

II. The District Court Entered Judgment of Noninfringement Based on No Multiple Logic Elements.

Dr. Hangartner filed his complaint in the Western District of Wisconsin, alleging that certain lines of Intel processors infringed claim 1 of the '422 patent. A52, A54-55. That court transferred the case to the District of Oregon, the judicial district in which Dr. Hangartner lives. A66, A363.

A. The District Court Construed Claim 1 to Require Synchronization of Multiple Logic Elements.

Early in the case, the parties identified a potentially dispositive noninfringement issue: the random number generation circuit of Intel's accused processors has only a single logic element. A87-88, A169.[2] A key issue during claim construction thus became whether claim 1 required synchronizing the operation of *multiple* logic elements. Dr. Hangartner proposed that "coupled to all of the … logic elements" in limitation (b) should be modified to mean "coupled to all of the *one or more* … logic elements." A77. Intel proposed that the phrase be construed as written, requiring multiple logic elements. *Id.*

The district court held a claim construction hearing and issued a ruling on November 20, 2014, followed by an explanatory opinion on December 17. A2-3, A4-19. Because the district court recognized that a requirement of multiple logic elements was likely dispositive, it focused

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[2] Dr. Hangartner appears to suggest (at 4) that the parties thought this issue would be dispositive for both sides. If so, he is incorrect. Intel has multiple claim construction arguments and noninfringement defenses in addition to those at issue in this appeal, and it has expressly preserved all such arguments. A169, A369. Intel's other defenses include invalidity based on the Bellido reference and other prior art.

largely on the phrase "coupled to all of the nondeterministic logic elements." A8-13.

The district court rejected Dr. Hangartner's proposal to read limitation (b) on a single-element circuit, construing it to mean "coupled to all of the *multiple* nondeterministic logic elements." A13. The court began its analysis with the express language of the claim. It observed that Dr. Hangartner had "deliberately pluralized 'logic elements'" multiple times in the "common synchronization means" limitation: the synchronization means was "coupled to 'all' of the logic 'elements' in order to synchronize the operation of the logic 'elements.'" A9. Dr. Hangartner had chosen to use the language "one or more" earlier in the claim, for different terms. A8. The court noted that Dr. Hangartner could have used similar language when he added limitation (b) during prosecution, "[h]ad he intended circuits comprised of only one logic element to fall within the scope" of that limitation. A10.

The district court addressed Dr. Hangartner's argument that limitation (a)'s reference to "one nondeterministic logic element" was somehow in tension with the plural language of limitation (b). A9. The court noted that "[t]his linguistic shift may be explained in part by the prose-

cution history": Dr. Hangartner added the "common synchronization means" limitation to overcome a rejection of a claim without the "common synchronization means." A10. When Dr. Hangartner later argued to the BPAI that his amended claim was patentable, he emphasized this limitation as an essential component of the claim. A11. The court found that the prosecution history was consistent with the plain meaning of the plural "logic elements" language, as it indicated that "Dr. Hangartner understood the final invention to include both one logic element for each variable as well as a means of synchronizing the operation of multiple logic elements within the circuit." *Id.*

B. The District Court Entered a Stipulated Judgment of Noninfringement Based on the Accused Products' Lack of Multiple Logic Elements.

Dr. Hangartner conceded that Intel's accused products did not infringe if claim 1 required multiple logic elements. Thus, the parties filed a Joint Stipulation for Entry of Final Judgment, stipulating to noninfringement in view of the court's construction of limitation (b) "as requiring multiple nondeterministic logic elements." A368. The district court entered final judgment of noninfringement in favor of Intel on January 5, 2015. A1. This appeal followed.

SUMMARY OF ARGUMENT

The district court's careful and complete analysis is correct that the claimed "common synchronization means coupled to all of the … logic elements" requires multiple logic elements. That conclusion follows from the plain meaning of the plural phrase "logic elements" and the terms "all of the," "common," and "synchronization." The court's construction is also confirmed by the prosecution history, where Dr. Hangartner added limitation (b) to overcome a rejection over a claim with language identical to limitation (a). It is further confirmed by the specification, which fails to disclose any single-element embodiments and describes the claimed "synchronizing operation of the … logic elements" as simultaneously triggering multiple logic elements to generate random values.

Dr. Hangartner's argument that the singular language of limitation (a) should control limitation (b) ignores the context of the overall claim. Limitation (a) provides that each logic element generates a value for a corresponding problem variable and describes the components of "each" element; limitation (b) provides that there are multiple such logic elements and that they must all be synchronized. As Dr. Hangartner

clarified during prosecution, this "common synchronization" among logic elements ensures that values are simultaneously generated for all variables in a problem. To the extent any tension exists between limitations (a) and (b), the tension is resolved by Dr. Hangartner's choice to add this unambiguously plural language during prosecution and the fact that limitation (b) was sufficient to overcome the rejection. The more specific language, which was necessary for patentability, must control.

ARGUMENT

I. The District Court Correctly Construed "Coupled to All of the … Logic Elements" to Require Multiple Logic Elements and Correctly Entered Judgment of Non-infringement on That Basis.

The Court should affirm the district court's construction of "coupled to all of the nondeterministic logic elements," because that construction is compelled by the plain language of the claim, the prosecution history, and the specification.

A. The Plain Language of Claim 1 Requires Multiple Logic Elements.

As Dr. Hangartner recognizes (at 20), the claim language itself is highly instructive. *See*, *e.g.*, *Vitronics Corp. v. Conceptronic, Inc.*, 90

F.3d 1576, 1582 (Fed. Cir. 1996) ("First, we look to the words of the claims themselves … to define the scope of the patented invention."). In this case, the plain language of limitation (b) unambiguously requires multiple elements.

1. "Logic Elements" Is Plural.

The "common synchronization means" limitation expressly recites that the claimed circuit includes multiple "logic elements." It uses this language twice, reciting that the synchronization means is coupled to "all of the nondeterministic logic elements" and that it "synchroniz[es] operation of the nondeterministic logic elements." This phrasing is clear, simple, and decisively plural.

Had Dr. Hangartner intended to claim "one or more" logic elements, as he now contends, he certainly could have done so. Indeed, he used such "one or more" language for other terms earlier in the claim. '422(12:56-57) ("one [or] more clauses in said one or more variables"). But he did not do so with "logic elements" in limitation (b), or, in fact, elsewhere. While Dr. Hangartner dismisses this analysis (at 15) as "linguistic," he also admits (at 20, citing *Neomagic Corp. v. Trident*

Microsystems, Inc., 287 F.3d 1062, 1075 (Fed. Cir. 2002)) that it is exactly such fidelity to the claim language that the Court requires.

2. The Language of Limitation (b) Indicates Multiple Elements: "*Common* Synchronization Means," "*Synchronizing* Operation of the … Elements," "Coupled to *All of The* … Elements."

Limitation (b)'s plural language is not the only claimed indicator of multiple logic elements. Other words and phrases within limitation (b) show that the claim requires multiple elements.

Claim 1 recites a "*common* synchronization means." In both ordinary English and electrical engineering parlance, "common" refers to something being shared among multiple subjects. *See, e.g.*, *Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1397 (Fed. Cir. 2008) (referring to a specification shared between patents as a "common specification"); *Linear Tech. Corp. v. ITC*, 566 F.3d 1049, 1055 (Fed. Cir. 2009) (observing that the "[asserted] patent's specification expressly discloses that the [claimed] 'second circuit' and 'third circuit' can share common components"). In Claim 1, the "synchronization means" is "common" to, or shared among, "all of the" logic elements. There is no way to give meaning to the term "common" in the context of a single logic element circuit.

Similarly, the very idea of "synchronizing" is inconsistent with a single-element circuit. Dr. Hangartner suggests (at 17) that "synchronization" refers only to "keep[ing] however many logic elements as may be in the circuit operating properly." He contends (at 17-18) that the '422 patent shows synchronization signal **32** generating control signals that control operation of the transistors inside the logic elements, and that these internal control signals must be synchronized to ensure that each logic element "operate[s] properly." This, Dr. Hangartner asserts, is what the claim means by "synchronization."

However, synchronization necessarily involves coordination between different entities. It makes no sense to "synchronize" one element or process with itself. Nor does it make sense to argue, as Dr. Hangartner does (at 17) that "synchronizing the operation of all of the nondeterministic logic elements" simply means making sure each element is "operating properly" on its own. Instead, "synchronizing operation of all of the … logic elements" means coordinating each logic element's operation with the operation of all other logic elements, such that the logic elements act simultaneously, as a unit, in generating a set of random values. *See, e.g.*, *Motorola Mobility, LLC v. ITC*, 737 F.3d

1345, 1349 (Fed. Cir. 2013) (the ordinary meaning of a "'synchronization component configured to synchronize' (certain objects with other objects)" in a mobile device "requires something more than whatever software may be needed simply for the mobile device to operate at all"); *Univ. of Pittsburgh v. Varian Med. Sys., Inc.*, 561 Fed. App'x 934, 936 (Fed. Cir. 2014) (invention's function of "synchronizing a radiation treatment beam with a patient's movements" meant, "[i]n other words, the radiation beam will turn on and off in synchronicity with the patient's breathing").

Dr. Hangartner's treatment of "synchronization" is also contrary to his chosen claim language and his statements during prosecution. Claim 1 recites "synchronizing operation *of the nondeterministic logic elements*," not "synchronizing operation *of components within*" each logic element or "synchronizing *internal* operation" of a logic element. And during prosecution, Dr. Hangartner emphasized to the PTO that the point of "synchronization" was that "each guess at a solution to the problem requires that a random value be picked *for every variable* in the problem." A220 (emphasis added). It is not enough for each element to be "operating properly," viewed alone; that is at least implicit in limita-

tion (a)'s description of the characteristics of a representative element. "Common synchronization" is instead needed to produce "each guess," because all logic elements must be told, at the same time, to generate the random values that collectively make up that guess.

In addition to being wrong about what "synchronization" means, Dr. Hangartner's position is factually inaccurate. Dr. Hangartner conflates synchronization signal **32** and the signals internal to each logic element. But this is incorrect—signal **32** is not singularly responsible for the "control signals" to the logic elements' internal components. Rather, as Figure 6 of the '422 patent shows, these internal signals are generated by a combination of signals—/RUN **66**, /FLIP **32**, ND/~FF **300**—and various logical operations.

The phrase "all of the" logic elements further indicates that the circuit of claim 1 must include multiple elements. This phrase would be superfluous under Dr. Hangartner's construction. There would be no need to specify that the synchronization means be coupled to "all of the" logic elements, if the circuit included only one element. *E.g.*, *Merck & Co. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A

claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

3. Limitations (a) and (b) Are Consistent.

Dr. Hangartner's single-element argument depends entirely on his theory that the reference to "one nondeterministic logic element" at the start of the limitation (a) is inconsistent with the plural language of limitation (b). His proposed solution to this "inconsistency" (at 10) is that the singular language should control because it comes first.

As an initial matter, even if Dr. Hangartner were correct that limitations (a) and (b) are fundamentally inconsistent—a point that Intel disputes—simply picking one of the two limitations to be controlling would not resolve this inconsistency. Instead, claim 1 would be indefinite for failing to inform a person of ordinary skill in the art "about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). Under Dr. Hangartner's interpretation, claim 1 does not fulfill its public notice function because it does not provide guidance as to the number of logic elements required.

In fact, however, limitations (a) and (b) are consistent. Limitation (a) recites that each logic element generates a value for one variable of the computing problem: there is "one nondeterministic logic element for generating a respective random boolean value for each one of the said one or more variables." The specification similarly makes clear that "[o]ne ND element is provided for each probabilistic ble." '422(4:14-15). Limitation (b) then recites a common means for synchronizing the operation of *multiple* logic elements, each of which functions in the manner specified by limitation (a).

Taken together, limitations (a) and (b) provide that the claimed circuit includes multiple logic elements, and that each element generates a random value for a variable of the problem. As the district court recognized, the claim language "indicates that Dr. Hangartner understood the final invention to include both one logic element for each variable as well as a means of synchronizing the operation of multiple logic elements within the circuit." A11. The circuit may use fewer logic elements than it has, depending on the number of variables in a particular problem. For example, if the circuit ever has to deal with a simple, single-variable "coin flip," it may use a single one of its multiple logic

elements to generate a random binary guess for that single variable. But the fact remains that the patented circuit must *contain* multiple elements, even if they are not all used to solve a given problem.

Dr. Hangartner contends (at 20) that failing to allow for a single-element circuit would render meaningless the preamble's reference to a problem expressed as "one [or] more clauses in … one or more variables." But again, the claimed logic circuit can be used to solve single-variable problems even though it includes multiple logic elements. There is nothing inconsistent about using only some of the multiple logic elements for a particular computing problem. To the contrary, the specification discloses that the random-number generating function for each logic element can be toggled on or off, depending on the number of random variables needed for a particular problem. '422(7:14-45, 8:14-22).

Indeed, tailoring the number of logic elements used for a specific problem is the only way the claimed circuit could generate guess solutions for its targeted complex, multi-variable problems as well as single-variable ones. Under Dr. Hangartner's construction, on the other hand, a single-logic element circuit would satisfy the claim even though it

would be incapable of solving the complex computing problems the invention was intended to solve. *See* A219 ("The invention … [is] specially configured to solve certain types of difficult (technically called 'NP-complete') computing problems."); '422(3:60-63) ("The present invention is most useful for solving a combinatorial computing problem having a large number of variables."). A construction with that result cannot be correct. *See, e.g.*, *CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1160 (Fed. Cir. 1997) ("In construing claims, the problem the inventor was attempting to solve, as discerned from the specification and the prosecution history, is a relevant consideration.").

4. There is No "Antecedent Basis" Issue.

In his arguments to this Court, Dr. Hangartner adds a new version to his single-element argument, now phrasing it in terms of "antecedent basis." To begin with, that argument was not preserved below, and the Court need not address it. *See Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1358 (Fed. Cir. 2006) ("a party may not introduce new claim construction arguments on appeal"). In any event, it is flawed in multiple ways.

Dr. Hangartner argues (at 9, 12, 13, 15) that the "the logic elements" language refers back to the phrase "one or more logic elements" recited earlier in the claim. On that basis, he contends, "logic elements" was introduced as being singular *or* plural and should be read as shorthand for "one or more." But claim 1 never recites "one or more logic elements." The claim refers to "one or more *variables*" in "one [or] more *clauses*," but it never uses the "one or more" language with respect to *logic elements*. The immediately antecedent reference to logic element(s) is "each logic element" in the description of a representative logic element, and "each" means every one of two or more. *E.g.*, *Alcohol Monitoring Sys., Inc. v. Actsoft, Inc.*, 414 Fed. App'x 294, 299 (Fed. Cir. 2011) (observing that "the plain meaning of 'each' is defined as 'being one of two or more distinct individuals having a similar relation and often constituting an aggregate'") (citation omitted). The antecedent is thus consistent with the plural nature of the common synchronization limitation.

In any event, as *Energizer Holdings, Inc. v. International Trade Commission*, 435 F.3d 1366 (Fed. Cir. 2006), cited by Dr. Hangartner at 11, explains, antecedent basis is a rule of patent drafting. It does not

independently affect the analysis of claim scope, which is determined by the claim language read in light of the specification. *Cf. id.* at 1370 ("When the meaning of the claim would reasonably be understood by persons of ordinary skill when read in light of the specification, the claim is not subject to invalidity upon departure from the protocol of 'antecedent basis.'").

Dr. Hangartner relies heavily (at 13, 15, 16) on *Baldwin Graphic Systems, Inc. v. Siebert, Inc.*, 512 F.3d 1338 (Fed. Cir. 2008). This reliance is misplaced. *Baldwin* cites the general grammatical rule that the "indefinite article 'a' or 'an' … carries the meaning of 'one or more'" in "open-ended" limitations. *Id.* at 1342. In *Baldwin*, the claim at issue recited "*a* pre-soaked fabric roll" and a "means for locating *said* fabric roll." *Id.* at 1340 (emphasis added). The district court construed "a presoaked fabric roll" to mean "a single presoaked fabric roll." *Id.* This Court held the construction to be in error, explaining that exceptions to the indefinite-article rule "are extremely limited: a patentee must 'evince[] a clear intent' to limit 'a' or 'an' to 'one.'" *Id.* at 1342 (citation omitted). Because the record contained no "clear indication that the

applicant departed from the general rule for the article 'a,'" this Court determined that the term was not limited to a single roll. *Id*. at 1343.

On *Baldwin*'s own terms, its rule—that "a" or "an" generally means "one or more"—does not apply to claim 1. Claim 1 never uses the indefinite articles "a" or "an" with respect to "logic element." The other modifiers of elements in the claim (with the exception of the cross-coupled inverter pair) are "each" and "the," which are definite determiners. There is simply no basis (in *Baldwin* or otherwise) to read the phrase "one or more logic elements" into claim 1. To the contrary, such a construction would be contrary to the language of the limitations, prosecution history, and specification—which, *Baldwin* expressly provides, limit the grammatical "one or more" rule. *Id*. Limitation (a) logically uses singular language to describe the characteristics of each representative element, and limitation (b) logically uses strictly plural language to specify that the circuit includes multiple such elements that are synchronized in common. Limitation (b)'s pluralization of "elements" is driven by the very nature of common synchronization.

To the extent Dr. Hangartner attempts to rely on the recent opinion in *TomTom, Inc. v. Adolph*, No. 2014-1699 (Fed. Cir. June 19, 2015),

that case is similarly inapposite. In *TomTom*, the claim recited "at least one storage device." Slip op. at 19. The panel determined that a later recitation of "the storage device" referred to "the 'at least one storage device' found in the first limitation" of the claim. *Id.* at 21. Again, and in contrast, claim 1 of the '422 patent does not recite "at least one" with respect to the logic elements. And as the *TomTom* Court noted, the overall claim language and specification are controlling over mechanical rules of grammar. *Id.* at 20-21.

The cases Dr. Hangartner cites for his antecedent basis argument stand for precisely what Intel is arguing: claim construction must be performed in the context of the claim language, prosecution history, and specification, not in isolation. There is no basis, grammatical or contextual, for rewriting limitation (b) to recite "one or more" logic elements.

B. Dr. Hangartner Added Limitation (b) to Overcome the Rejection of Limitation (a).

The prosecution history confirms why limitation (b) was worded in the plural and why Dr. Hangartner could not and did not patent a circuit with a single logic element.

1. Dr. Hangartner Consistently Referred to Plural "Logic Elements" When Characterizing Application Claim 10 During Prosecution.

Originally, Dr. Hangartner tried to patent a claim that did not include the "common synchronization means." A209-10. The examiner rejected that claim. A210. Rather than traversing the rejection, Dr. Hangartner attempted to overcome it by adding limitation (b), with its plural "logic elements" language. A209-10, A214.

Dr. Hangartner knew exactly what he meant by this language at the time, emphasizing to the PTO that the amended claim had "essentially two elements," including the "'common synchronization means' that synchronizes operation of the nondeterministic logic *elements*" (plural). A220 (emphasis added). He explained that "*[t]hey*"—the plural logic elements—"have to be synchronized because each guess at a solution to the problem requires that a random value be picked for every variable in the problem." *Id.* (emphasis added); *see also* A240 ("[i]n addition to the *nondeterministic structures* described in [application claim 10], it also describes a specific arrangement to tie the various *elements* together") (emphasis added).

Dr. Hangartner never described application claim 10 as including "one or more" logic elements. Instead, he consistently used plural language throughout prosecution to describe the synchronized logic elements. This indicates that he intended the "common synchronization means" limitation to refer to multiple logic elements, consistent with its plain language.

2. Under Dr. Hangartner's Construction, Limitation (b) Could Not Have Overcome the Double Patenting Rejection.

Dr. Hangartner now disputes the implications of the prosecution history, arguing (at 17) that the amendment "does nothing to suggest that 'more than one' logic element is required by the claim." According to Dr. Hangartner (at 13, 17), the "common synchronization means" merely "keep[s] however many logic elements as may be in the circuit operating properly" such that if the circuit includes only one logic element, only one element need be coupled to the "synchronization means."

But as Dr. Hangartner effectively conceded in his chosen response to the double-patenting rejection, a claim that recited only limitation (a)—a logic element that generates a random value—was not patentable. Adding a limitation that simply required this logic element to

"operate properly" could not have overcome the rejection. In fact, limitation (a) already required the logic element to "operate properly": it expressly recites that the latch and means components of the logic element work together to "provid[e] a probabilistically selected random boolean value." '422(12:66-13:8). If limitation (b) means what Dr. Hangartner now says it does, its addition would have contributed nothing of substance to the claim.

Dr. Hangartner's contention (at 19) that the invention of claim 1 is simply a machine for producing random values fails for similar reasons. If claim 1 were nothing more than a latch-based random number generator, the "special tool" used by the system of the other independent claims to solve a problem, it would have ended after reciting the components of the logic element that generate a random value. In other words, it would have included only limitation (a). But that truncated form is exactly what was rejected. Dr. Hangartner's addition of the "common synchronization means" was a concession that a claim drawn to nothing more than a logic element that generates random values—even one with the specific subcomponents recited by limitation (a)—was not patentable.

This explains Dr. Hangartner's arguments to the PTO, which consistently described *multiple* logic elements coupled to the common synchronization means. Dr. Hangartner represented to the PTO (at A220) that the added requirement of *synchronization* between *multiple* logic elements—synchronization to ensure that the elements would simultaneously and collectively generate a set of random values for every variable in the problem—was what merited patentability. The prosecution history confirms the plain meaning of the claim language: "logic elements" means element*s*, plural.

C. The Specification is Consistent with Limitation (b)'s Requirement of Multiple Logic Elements.

The specification is the "best source" for construing a claim term and determining the inventor's intent regarding use. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (quotation omitted). That remains true when determining whether a limitation requires one, one or more, or more than one of something. *See Insituform Techs., Inc. v. Cat Contracting, Inc.*, 99 F.3d 1098 (Fed. Cir. 1996). Consistent with the claim language and prosecution history, the specification of the '422 patent confirms that claim 1 requires multiple logic elements.

1. The Only Disclosed Embodiment Includes Multiple Elements.

The specification repeatedly and exclusively describes a circuit with multiple logic elements. *See*, *e.g.*, '422(2:37-41) ("The nondeterministic subsystem includes a series of semiconductor nondeterministic logic elements."); '422(7:1-5) ("The ND subsystem further includes a series of p individual ND logic elements **70** …."); Figure 4 (depicting series of logic elements **70**). Nowhere does the specification disclose a circuit with only a single logic element, and nowhere does Dr. Hangartner's brief address that fact. While this aspect of the specification might not itself limit claim language that otherwise claimed a single element circuit, the specification's disclosure is, as the district court noted, universally consistent with the plain plural language of the key limitation. A12-13.

This absence of any single-element embodiment is entirely logical: having multiple logic elements is fundamental to the invention of the '422 patent. The specification discloses that the computing system was meant to produce solutions for highly complex problems, potentially involving thousands of independent variables. '422(3:60-63). It does so by employing "a series of … logic elements," each generating a value for

one of the problem variables. '422(7:1-5). Dr. Hangartner repeatedly describes "the invention" in this manner. '422(3:60-63) ("*The present invention* is most useful for solving a combinatorial computing problem having a large number of variables."), A219 ("*The invention* can be briefly summarized as an electronic system specially configured to solve certain types of difficult (technically called 'NP-complete') computing problems.") (emphases added). This one-to-one correspondence between logic elements and variables, where each element generates a random value for a different variable of the invention's objective—a problem with many variables—is the only technique disclosed.

Relatedly, the only corresponding structure disclosed for the "common synchronization means" limitation is a signal directed to multiple logic elements. Dr. Hangartner agreed (*see* A77) that "common synchronization means" is a means-plus-function term subject to the requirements of 35 U.S.C. § 112 ¶ 6 (now 35 U.S.C. § 112(f)). He further agreed that the corresponding structure for the recited function of "synchronizing operation of the logic elements" is synchronization signal **32** (along with delay element **64**, which generates signal **32**). A77. But as Figure 4 of the '422 patent illustrates (*see supra* at 9), signal **32**

fans out to create a number of parallel control signals, one for each of the multiple logic elements. '422(7:8-11) ("DDELAY signal fans out … to form a series of control signals … each control signal being coupled to a corresponding one of the individual ND elements."). As discussed above, signal **32** "synchronizes" the logic elements by simultaneously triggering all of the logic elements to generate new random numbers. '422(6:66-67, 11:6-7).

The specification thus confirms that claim 1 means what it says: common synchronization of multiple logic elements.

2. A Circuit With Multiple Logic Elements Is Not Merely a "Preferred Embodiment."

Dr. Hangartner characterizes (at 18) the logic element's ability to solve complex computing problems as a "preferred embodiment." Citing *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898 (Fed. Cir. 2004), he complains that the district court improperly limited claim 1 based on this embodiment. But *Liebel-Flarsheim* does not support Dr. Hangartner. The claims at issue there were directed to methods of loading a replacement syringe into a high pressure power injector. *Id.* at 903. The accused infringer argued that because all embodiments described in the specification featured pressure jackets, the claims must be lim-

ited to devices that used pressure jackets. *Id*. at 905-06. The district court agreed, but this Court reversed. The Court pointed out that nothing in the claim language referred to or required a pressure jacket and the specification did not clearly disavow claim scope. *Id*. at 905-07. Further, during prosecution the applicants had expressly stated that their claims did not necessarily require a pressure jacket. *Id*. at 909. Based on the complete context—the claim language, specification, and prosecution history—the Court concluded that the district court had erred in construing the claims to require pressure jackets.

Here, by contrast, the complete context drives the opposite result. The requirement of multiple logic elements comes from the *claim language itself*. The prosecution history independently confirms that claim 1 must require multiple elements—otherwise, Dr. Hangartner's claim would have remained rejected. The fact that the specification is entirely consistent with the claim language and prosecution does not show that the district court limited the claim to a preferred embodiment. Rather—and as the district court observed (at A12-13)—it confirms that all of the intrinsic evidence is consistent with the district court's construction based on the language of the claim.

CONCLUSION

The Court should affirm the judgment of noninfringement.

Respectfully submitted,

PERKINS COIE LLP

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CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B). The brief contains 7,824 words, excluding the portions exempted by Federal Rule of Appellate Procedure 32(a)(7)(B)(iii).

2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6). The brief has been prepared in a proportionally spaced typeface using Microsoft® Word 2010 and 14-point Century Schoolbook type.

Dated: July 20, 2015.

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PROOF OF SERVICE

In accordance with Federal Rule of Appellate Procedure 25 and Federal Circuit Rule 25, I certify that I caused this brief to be served via the Federal Circuit's CM/ECF system on counsel of record for the appellant.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Dated: July 20, 2015.

/s/ David J. Burman
David J. Burman